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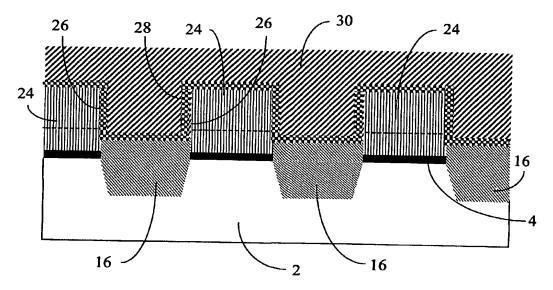
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[Continued on next page]

#### (54) Title: SHALLOW TRENCH ISOLATION IN FLOATING GATE DEVICES



(57) Abstract: The present invention provides a method for manufacturing a floating gate type semiconductor device on a substrate having a surface (2), and a device thus manufactured. The method comprises: - forming, on the substrate surface, a stack comprising an insulating film (4), a first layer of floating gate material (6) and a layer of sacrificial material (8), - forming at least one isolation zone (18) through the stack and into the substrate (2), the first layer of floating gate material (6) thereby having a top surface and side walls (26), - removing the sacrificial material (8), thus leaving a cavity (20) defined by the isolation zones (18) and the top surface of the first layer of floating gate material (6), and filling the cavity (20) with a second layer of floating gate material (22), the first layer of floating gate material (6) and the second layer of floating gate material (22) thus forming together a floating-gate (24).

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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01L27/115 H01L H01L21/8247 According to International Patent Classification (IPC) or to both national classification and IPC **B. FIELDS SEARCHED** Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01L Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal C. DOCUMENTS CONSIDERED TO BE RELEVANT Category ° Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No. X US 6 391 722 B1 (KOH CHAO-MING) 1,2,4, 21 May 2002 (2002-05-21) 6-10 the whole document X US 6 222 225 B1 (ARAI FUMITAKA ET AL) 1-4,6,24 April 2001 (2001-04-24) 8-10 column 5, line 6 - column 6, line 16; figures 5a-5h χ US 2002/093073 A1 (NOGUCHI MITSUHIRO ET 1.4.6. AL) 18 July 2002 (2002-07-18) 8-10 paragraph '0051! - paragraph '0059!; figures 3a-4c Further documents are listed in the continuation of box C. Patent family members are listed in annex. Special categories of cited documents: "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the "A" document defining the general state of the art which is not considered to be of particular relevance invention "E" earlier document but published on or after the international "X" document of particular relevance; the claimed invention filing date cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled "O" document referring to an oral disclosure, use, exhibition or other means document published prior to the international filing date but later than the priority date claimed in the art. \*&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the International search report 25 June 2004 02/07/2004 Name and mailing address of the ISA Authorized officer European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016 Baillet, B

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